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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,212	05/31/2001	Omar Kebichi	1011-58140	1993

7590 01/06/2005

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,212	KEBICHI ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on th cover sheet with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30,32 and 34-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30,32 and 34-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *20041226* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

FINAL OFFICE ACTION

0. This office action is in response to Applicants' Amendment of 6/10/04.

0.1 The Examiner gratefully acknowledges Applicants' cooperation in trying to expedite prosecution of instant application. The proposed amendment of 23 Dec. 2004, however, does not place current claims in condition for allowance.

0.2 **Claims 31, 32** (2nd occurrence) and **33** are cancelled; **Claims 30, 32** (1st occurrence), **35-36 are** amended; **Claim 37** is added. **Claims 1-30, 32, 34-37** remain pending.

0.3 The prior art rejections to the claims of record are maintained in response to Applicants' Amendments.

0.4 All remaining objections of record are withdrawn in response to Applicants' Amendments.

Response to Arguments

1. Applicants' arguments have been fully considered, but they are not found persuasive.

REMARKS

2. In response to **Claims 1-30, 32, 34-37**, Applicants argue, on page 8 para. 2 et seq., that the prior art of record does not teach the claimed invention, i.e., a resume pin that causes plural controllers to exit an idle state.

Examiner disagrees because the **admitted prior art Fig. 1** discloses a testing system wherein an automatic test equipment sequences plural memory testing tasks, such as activating a hold or pause or idle state in testing operations followed by a continue or resume state activation in testing operations via plural control means, such as hold pins, to plural BIST controllers.

Examiner notes that the claimed invention is a subset of admitted prior art **Fig. 1**: in sequential mode, the ATE activates the hold/idle/pause pin/terminals individually. However, in parallel mode the ATE activates the hold/idle/pause pin/terminals simultaneously. **Therefore,** in

sequential mode, hold/idle/pause pin/terminals are distinguishably separate while in parallel mode, such hold/idle/pause pin/terminals are just a single pin.

Examiner also notes that a hold pin and resume pin perform mutually exclusive functions, i.e., when the hold pin is asserted, the resume pin is disabled and vice versa in a manner similar to a toggle switch.

Examiner further notes that, in a sequential mode, sync means is provided by ATE to issue idle and hold commands to sequence individually through each of the plural controllers for testing tasks to proceed without timing contention. Thus, a hold pin and resume pin perform mutually exclusive functions wherein a 1st controller is put in idle state at appropriate timing followed by a 2nd controller, hitherto in idle state, entering a resume state under ATE control. Thus when the hold pin is asserted, the resume pin is disabled and vice versa so as to ensure proper testing synchronization.

In other words, the claimed invention carves out the above parallel mode of the admitted prior art **Fig. 1** and recites inherent synchronization means necessary in digital circuit operation.

2.1 In response to **Claims 1-30, 32, 34-37**, Applicants also argue, on page 11 last para. et seq., that the prior art of record does not teach the claimed invention, i.e., a circuit having at least one BIST controller within an integrated circuit.

Examiner disagrees because the **admitted prior art Fig. 1** discloses a testing system wherein controllers 18 are embedded in IC 14 under sync control of ATE 12.

Examiner also notes that an idle state is a hold state. Therefore a key word search of 'idle state' excluding 'hold or pause state' may return zero as alleged by applicants on page 12 1st para.

Claim Rejections - 35 USC ' 102

3. **Claims 1-3, 8, 12** are rejected under 35 U.S.C. 102 (e) as being unpatentable over **Applicants' admitted prior art.**

As per Claims 1-3, 8, 12, Applicants admit as prior art the claimed IC with BIST arrangement comprising plural BIST controllers, resume/hold input external/internal pins or terminals, ATE coupling means, idle state means (page 3 line 21) and memory composed of DRAM or SRAM or ROM in **prior art** Fig. 1 and related description.

Claim Rejections - 35 USC ' 103

4. **Claims 4-7, 9-11, 13-30, 32, 34-37** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Phan** (US Patent No. 6651202).

As per Claims 4-7, 9-11, 13-30, 32, 34-37, Admitted prior art substantially discloses the claimed IC with BIST arrangement comprising plural BIST controllers, resume input external/internal pins or terminals, ATE coupling means, idle state means (page 3 line 21) and memory composed of DRAM or SRAM or ROM, IDDQ/walking/testing means in **prior art** Fig. 1 and related description.

Not specifically described in detail in Admitted prior art is the step of state machine controlling means for synchronization.

However, such state machine controlling means is well known. **For example, Phan,** in an analogous art, discloses a **BIST arrangement** in Fig. 1: BLOCK 102 and related description.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Admitted prior art** by including therein state machine controlling means OPERATION TIMING for each of **plural BIST controllers**, as taught by **Phan,** because such modification would provide the procedure

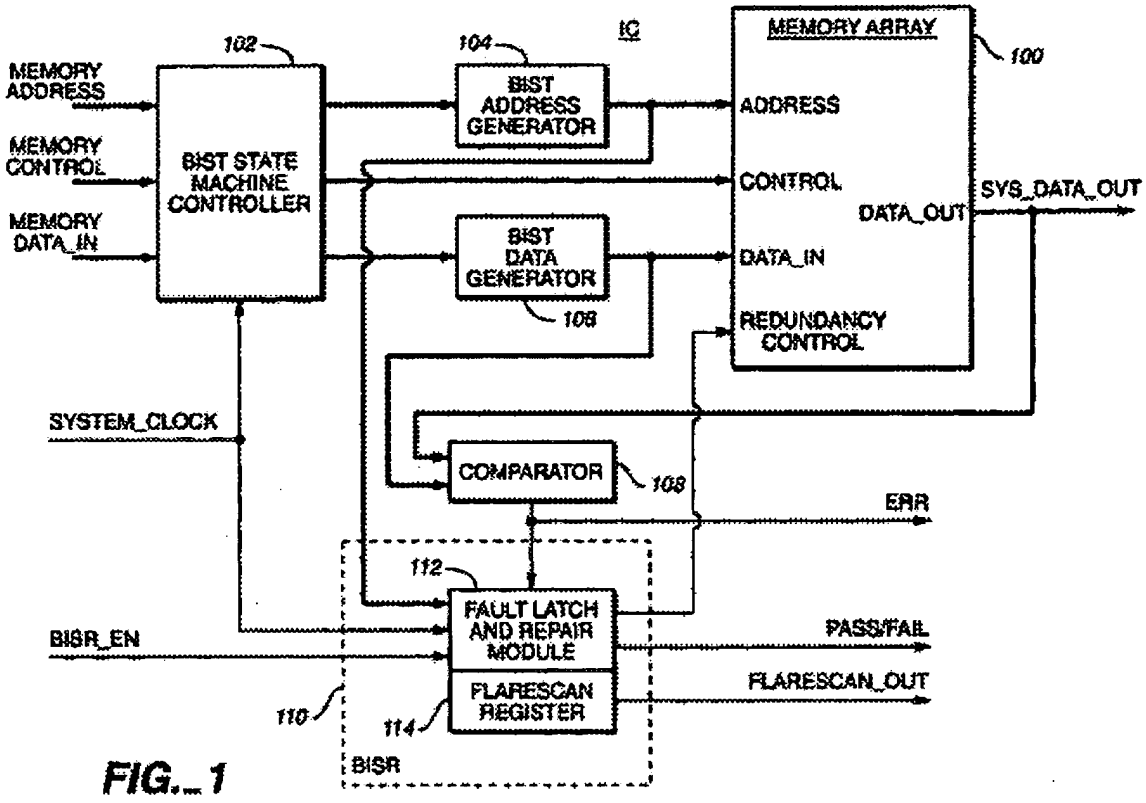

FIG._1

disclosed in **Admitted prior art** with a technique whereby "*The outputs of the BIST address generator 104 thereby control the address inputs of the memory array 100 during execution of a test pattern algorithm. Thus, the BIST address generator 104 and BIST data generator 106 may provide address and data sequences, respectively, to the memory array 100 in an order as specified by a test pattern algorithm. Preferably, such sequences provide a set of data bits in a pattern that maximizes fault coverage for detecting various types of faults within the memory array 100. A system clock signal SYSTEM_CLOCK is also provided to both the BIST state machine controller 102 and the BISR circuitry 110 for logic clocking and synchronization.*" {See **Phan,** col. 4 line 29 et seq.}

4.1 Claims 4-7, 9-11, 13-30, 32, 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Huang et al.** (US Patent No. 6,415,403; Jan. 29, 1999).

As per Claims 4-7, 9-11, 13-30, 32, 34-37, Admitted prior art substantially discloses the claimed IC with BIST arrangement and HDL means therefor comprising plural BIST controllers, resume input external/internal pins or terminals, ATE coupling means, idle state means (page 3 line 21) and memory composed of DRAM or SRAM or ROM, IDDQ/walking/testing means in **prior art** Fig. 1 and related description.

Not specifically described in detail in Admitted prior art is the step of state machine controlling means for synchronization.

However, such state machine controlling means is well known. **For example, Huang et al.,** in an analogous art, discloses a **BIST arrangement** In Figs. 3-4 and related description. **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in **Admitted prior art** by including therein state machine controlling means OPERATION TIMING for each of **plural BIST controllers**, as taught by **Huang et al.,** because such modification would provide the procedure disclosed in **Admitted prior art** with a technique whereby "When the BAC control signal is high, a logical one, the BIST circuit is activated to test the embedded memory 13. All signals are synchronized with the BIST clock, BCK. The BRS signal is pulled high along with BCS at the beginning of the BAC control signal to perform a scan test to verify that the BIST controller is operating correctly. Scan chains are formed between BSI and BSO to apply patterns and collect responses. When the scan test is completed the BRS signal is pulled low to reset the BIST controller, and BCS remains low to generate a reset sequence. The BRD and BGO signal are also brought low, and the BIST controller performs a scan test for the remainder of the BIST circuitry. Once the scan test is completed, a test algorithm is applied to the embedded DRAM 13 in accordance with the control sequence of the finite state machine shown in FIG. 2. At the end of the test sequence BRD is brought high and BGO is sampled to read out the test results. Then BAC is set to a low

state to return the DRAM 13 to normal operations. " {See **Huang et al.,** FIG. 3 and related description.}

Conclusion

5. THIS ACTION IS MADE FINAL. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
12/26/04